UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/589,621	06/07/2000	Sara Ruhina Biyabani	004860.P2438	8620

7590 04/01/2008

Sheryl Sue Holloway
Blakely Sokoloff Taylor & Zafman LLP
12400 Wilshire Boulevard 7th Floor
Los Angeles, CA 90025

EXAMINER	
CASCHERA, ANTONIO A	
ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
04/01/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/589,621	BIYABANI, SARA RUHINA	
	Examiner	Art Unit	
	Antonio A. Caschera	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-9,11-14,16-21 and 23-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-9,11-14,16-21 and 23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 2-9, 11-14, 16-21 and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stortz (U.S. Patent 5,900,885) in view of Priem et al. (European Patent 0525986).

In reference to claim 2, Stortz discloses a video memory architecture including a system memory controller connected via a bus to a system memory, a CPU and to a video buffer in video memory (see Figure 1 of Stortz, System Memory Controller (#15) connects to CPU (#12), memory (#14) via bus (#18) along with video DRAM (#22) and Figure 2, #14, #22, #42a and #42b). Stortz discloses assigning an incremental video buffer in main memory and a dedicated video buffer in video memory (see Figure 2, #42a, 42b and column 2, lines 41-44). Note, the Office interprets the incremental video buffer in main memory functionally equivalent to the frame-preparation memory and dedicated video buffer functionally equivalent to the refresh memory of Applicant's claim. Stortz explicitly discloses using the system memory controller to control both incremental video buffer in main memory and the video buffer in video memory (see column 1, lines 61-64 and column 3, lines 13-16). Note, with Stortz explicitly disclosing the system memory controller coupled to CPU (#12 of Figure 1), main memory (#14) and video

memory (#22) along with the controlling of both main memory and video memory by the system memory controller therefore allows the Office to interpret that Stortz manages the use of the main memory between a graphics subsystem (video controller #20 of Figure 1) and a processing unit (CPU #12 of Figure 1). Further, Stortz explicitly discloses that the allocation of main memory to an incremental video buffer is performed by a modification of the system memory controller (see column 2, lines 54-57), therefore the Office interprets that the system memory controller of Stortz is "operable" for partitioning an address space for the color buffer (since video buffers are used in Stortz, they inherently comprise of color data and are therefore interpreted as equivalent to "color buffers"). Stortz also discloses connecting the incremental video buffer to a graphics subsystem and connecting the video buffer to a display device (see column 1, lines 44-53, column 3, lines 2-6, Figure 1, Memory (#14) is connected to Video Controller (#20) via bus (#18) and DRAM (#22) is connected to Display (#24) and see Figure 2, reference #42a, #42b). Stortz also discloses that a portion of incremental video buffer is copied to and received by a look-ahead video buffer, found within the graphics subsystem of Stortz, while a portion of data is read out from dedicated video buffer to a display device (see column 3, lines 2-6, Figure 1, #20, 22, 24 and Figure 2, #22, 42a, 42b, 44). Although Stortz does disclose the incremental and dedicated video buffers to store video data (see column 2, lines 62-64), Stortz also discloses them functioning in an interleaved storing manner in one embodiment and in an alternate embodiment discloses the invention to function without interleaving (see column 3, lines 16-17). However, Stortz still does not explicitly disclose storing a full frame of data within the buffers and operating upon a frame rate when writing full frames of data to the buffers. Priem et al. discloses methods and apparatus for eliminating frame tearing from a

computer output display through the use of inexpensive double buffering (see column 1, lines 5-10). Priem et al. discloses the apparatus to comprise in an embodiment, of two VRAM buffers and in another embodiment of one frame buffer (VRAM) and one DRAM buffer (see column 6, lines 47-52) serving as the memories in the double buffering scheme. Priem et al. also explicitly discloses writing a frame of data to the frame buffers and multiplexing a frame of data from one of the buffers to the display (see column 6, lines 20-24, 31-34 and Figure 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the full frame double buffered memory writing, reading and timing techniques of Priem et al. with the video buffering techniques of Stortz in order to ensure the correct displaying of data on a display of a computing device by prohibiting the occurrence of frame tearing since data is never written to a frame buffer while its contents are being sent to the display device (see column 6, lines 35-37 of Priem et al.).

In reference to claim 3, Stortz and Priem et al. disclose all of the claim limitations as applied to claim 2 above. Stortz discloses that a portion of incremental video buffer is copied to and received by a look-ahead video buffer, found within the graphics subsystem of Stortz, while a portion of data is read out from dedicated video buffer to a display device (see column 3, lines 2-6, Figure 1, #20, 22, 24 and Figure 2, #22, 42a, 42b, 44).

In reference to claims 4, 13, 17 and 25, Stortz and Priem et al. disclose all of the claim limitations as applied to claims 3, 11, 16 and 23 respectively above in addition, the Office interprets that the system memory controller of Stortz inherently copies data from the incremental video buffer, in main memory to the dedicated video buffer in the graphics subsystem at "pre-determined intervals" since "portions" of data are copied at a time and

"portions" of data are sent to a display from the video memory. In other words, such a broad term, "pre-determined intervals" is inherently found in the double-buffering techniques of Stortz at each time a new "portion" of video data is required to be displayed.

In reference to claims 5, 12, 18 and 24, Stortz and Priem et al. disclose all of the claim limitations as applied to claims 3, 11, 16 and 23 respectively above. The Office interprets that since Stortz discloses that a portion of incremental video buffer is copied to and received by a look-ahead video buffer, found within the graphics subsystem of Stortz, while a portion of data is read out from dedicated video buffer to a display device (see column 3, lines 2-6, Figure 1, #20, 22, 24 and Figure 2, #22, 42a, 42b, 44), the incremental video buffer operates based upon a frame rate and therefore copies data when an entire frame is ready for further processing/display. Even further, Priem et al. discloses transferring frames of data from DRAM to VRAM buffers when new data is written to the DRAM buffer, a frame is transferred to VRAM buffer (see column 8, lines 2-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the full frame double buffered memory writing, reading and timing techniques of Priem et al. with the video buffering techniques of Stortz in order to ensure the correct displaying of data on a display of a computing device by prohibiting the occurrence of frame tearing since data is never written to a frame buffer while its contents are being sent to the display device (see column 6, lines 35-37 of Priem et al.).

In reference to claims 6, 14 and 19, Stortz and Priem et al. disclose all of the claim limitations as applied to claims 1, 11 and 16 respectively above. Stortz discloses a portion of incremental video buffer is copied to and received by a look-ahead video buffer, found within the graphics subsystem of Stortz, while a portion of data is read out from dedicated video buffer to a

display device (see columns 2-3, lines 67-12, Figure 1, #20, 22, 24 and Figure 2, #22, 42a, 42b, 44). Note, the Office interprets the third-logical buffer of Applicant's claims equivalent to the look-ahead buffer of Stortz.

In reference to claims 7 and 20, Stortz and Priem et al. disclose all of the claim limitations as applied to claim 6 and 19 respectively above. Stortz discloses that a portion of incremental video buffer is copied to and received by a look-ahead video buffer, found within the graphics subsystem of Stortz, while a portion of data is read out from dedicated video buffer to a display device (see columns 2-3, lines 67-12, Figure 1, #20, 22, 24 and Figure 2, #22, 42a, 42b, 44). Stortz further discloses that the next portion of data is read directly from the look-ahead buffer, instead of system memory, and received by the dedicated video buffer (see column 3, lines 6-8). Therefore, the Office interprets Stortz discloses such "disconnection" of the system memory from the graphics subsystem as the role of the look-ahead buffer is switched to the frame-preparation memory (previously known as the incremental video buffer located in system memory).

In reference to claims 8 and 21, Stortz and Priem et al. disclose all of the claim limitations as applied to claims 7 and 20 respectively above. The Office interprets that since Stortz discloses that a portion of incremental video buffer is copied to and received by a look-ahead video buffer, found within the graphics subsystem of Stortz, while a portion of data is read out from dedicated video buffer to a display device (see column 3, lines 2-8, Figure 1, #20, 22, 24 and Figure 2, #22, 42a, 42b, 44), the incremental video buffer operates based upon a frame rate and therefore copies data when an entire frame is ready for further processing/display. Stortz explicitly discloses, "After this local data is read, the next portion of display data is read

directly from look-ahead video buffer…" (see column 3, lines 6-8). Even further, Priem et al. discloses transferring frames of data from DRAM to VRAM buffers when new data is written to the DRAM buffer, a frame is transferred to VRAM buffer (see column 8, lines 2-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the full frame double buffered memory writing, reading and timing techniques of Priem et al. with the video buffering techniques of Stortz in order to ensure the correct displaying of data on a display of a computing device by prohibiting the occurrence of frame tearing since data is never written to a frame buffer while its contents are being sent to the display device (see column 6, lines 35-37 of Priem et al.).

In reference to claim 9, Stortz and Priem et al. disclose all of the claim limitations as applied to claim 2 above. Stortz discloses assigning an incremental video buffer in main memory and a dedicated video buffer in video memory (see Figure 2, #42a, 42b and column 2, lines 41-44). Note, the Office interprets the incremental video buffer in main memory functionally equivalent to the frame-preparation memory and dedicated video buffer functionally equivalent to the refresh memory of Applicant's claim. Stortz explicitly discloses using the system memory controller to control both incremental video buffer in main memory and the video buffer in video memory (see column 1, lines 61-64 and column 3, lines 13-16). Priem et al. discloses a multiplexer switching the designation of frame buffers to the display device so that when a frame of data has been completely written to a frame buffer, the data in that frame buffer may in turn be scanned to the display and new data may be written to the other frame buffer (see column 6, lines 17-25, 31-37, #14, 16, 17, 19 of Figure 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the full frame double

buffered memory writing, reading and timing techniques of Priem et al. with the video buffering techniques of Stortz in order to ensure the correct displaying of data on a display of a computing device by prohibiting the occurrence of frame tearing since data is never written to a frame buffer while its contents are being sent to the display device (see column 6, lines 35-37 of Priem et al.).

In reference to claim 11, claim 11 is equivalent in scope to claim 2 and is therefore rejected under similar rationale. The Office further notes that claim 11 is a "method" type claim and that the combination of Stortz and Priem et al. teach the method steps as recited in claim 11.

In reference to claim 16, claim 16 is equivalent in scope to claim 2 and is therefore rejected under similar rationale.

In reference to claim 23, claim 23 is equivalent in scope to claim 2 and is therefore rejected under similar rationale. Further, the Office interprets the combination of Stortz and Priem et al. to disclose preparing a "full" frame of color data for display since Priem et al. discloses a multiplexer switching the designation of frame buffers to the display device so that when a frame of data has been completely written to a frame buffer, the data in that frame buffer may in turn be scanned to the display and new data may be written to the other frame buffer (see column 6, lines 17-25, 31-37, #14, 16, 17, 19 of Figure 1).

In reference to claim 26, Stortz discloses all of the claim limitations as applied to claim 23 above. Claim 26 is equivalent in scope to the combination of claims 5-8 and is therefore rejected under similar rationale.

Response to Arguments

2. Applicant's arguments filed 01/14/2008 have been fully considered but they are not persuasive.

In reference to claims 2-9, 11-14, 16-21 and 23-26, Applicant argues that the combination of Stortz and Priem is improperly motivated since there is no motivation to replace the buffers of Stortz with the buffers of Priem because Priem explicitly teaches that a single memory controller system cannot keep up with a frame rate required by a display thus teaching away from using a single memory controller system (see pages 9-10 of Applicant's Arguments).

In response to Applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, both Stortz and Priem are concerned with and disclose buffering techniques between system and graphics memories. Stortz discloses a method and system for controlling a composite buffer, created from multiple separate buffers located within system and video memories (see column 1, lines 39-43) while Priem discloses a double buffering output display system that uses multiple frame buffers, the frame buffers being of VRAM and DRAM type memory, in displaying data (see column 6, lines 1-58). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the buffering of full frame data of Priem with the video buffering techniques of Stortz in order to ensure the correct displaying of data on a display of a computing device by displaying one full frame of data at a

time, thereby ensuring that a full complete viewable screen of data is shown to the user. Further, with reference to Applicant's explicit arguments above, the Office firmly disagrees with Applicant's arguments and states that the motivation for combining the full frame operation techniques including buffers of Priem with the video buffering system of Stortz is exactly brought about by Applicant's arguments. In particular, operating (reading/writing) with full frames of data in Stortz would aid in ensuring that frame tearing would not occur since only when complete/entire frames of data are processed would further data be processed. The fact that Priem discloses utilizing two controllers does not affect the reasoning of operating upon full frames of data in a display system such as the one disclosed by Stortz. Therefore, the Office maintains its rejection based upon Stortz and Priem.

Even further, Applicant argues that the combination of Stortz and Priem does not disclose each claim limitation, in particular, that neither Stortz nor Priem disclose the frame buffers mapped into main memory (see page 10 of Applicant's Remarks).

In response, the Office disagrees and points to the above rejection of the claims. In particular, the Office has established that Stortz does actually disclose such limitations wherein Stortz discloses assigning an incremental video buffer in main memory and a dedicated video buffer in video memory (see Figure 2, #42a, 42b and column 2, lines 41-44). Note, the Office interprets the incremental video buffer in main memory functionally equivalent to the frame-preparation memory and dedicated video buffer functionally equivalent to the refresh memory of Applicant's claim. Even further however, Priem discloses the apparatus to comprise in an embodiment, of two VRAM buffers and in another embodiment of one frame buffer (VRAM) and one DRAM buffer (see column 6, lines 20-24, 31-34 and 47-52) serving as the memories in

the double buffering scheme. Priem et al. also explicitly discloses writing a frame of data to the frame buffers and multiplexing a frame of data from one of the buffers to the display (see column 6, lines 20-24, 31-34 and Figure 1). It can be seen from Priem that VRAM or video random access memory is video memory and therefore can be interpreted by the Office that the alternate DRAM buffer is not video memory. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the buffering of full frame data of Priem with the video buffering techniques of Stortz in order to ensure the correct displaying of data on a display of a computing device by displaying one full frame of data at a time, thereby ensuring that a full complete viewable screen of data is shown to the user. The Office maintains its rejection based upon Stortz and Priem.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Antonio Caschera whose telephone number is (571) 272-7781. The examiner can normally be reached Monday-Thursday and alternate Fridays between 7:00 AM and 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung, can be reached at (571) 272-7794.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

571-273-8300 (Central Fax)

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (571) 272-2600.

/Antonio A Caschera/

Examiner, Art Unit 2628

3/31/08

/Kee M Tung/

Supervisory Patent Examiner, Art Unit 2628